

Model Name: P35-DS3P 1.01

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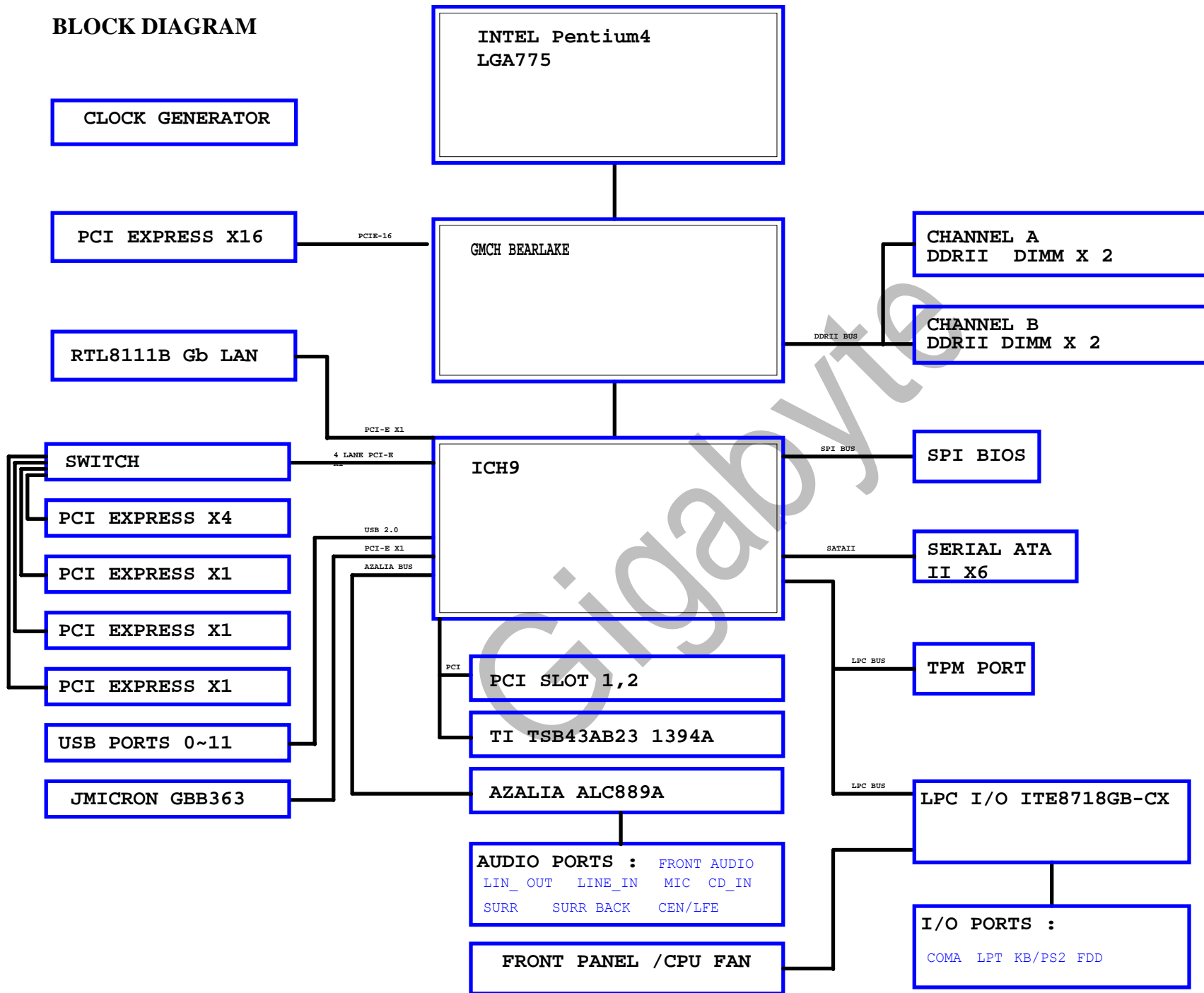
SHEET TITLE

28	DUAL BIOS
29	ALC889
30	REAR AUDIO JACK
31	VCORE PWM_ISL6327CRZ-1
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37	FP,FUSB,FDD
38	TI TSB43AB23 1394
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Component value change history

BLOCK DIAGRAM



LOW

ICH9 GPIO LIST TABLE

PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	VTT_GMCH_OV3	
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	DDR18V_OV4	
GP9	STBY	H-Z	GPIO9(DUALBIOS_INPUT)	
GP10	STBY	H-Z	DDR18V_OV5	P/D 100K GND/X
GP11/SMBALERT#	STBY	NATIVE	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	L OUT	AUDIO DETECT	P/U 8.2K VCC3
GP13	STBY	L IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	H-Z	DDR18V_OV2	P/U 8.2K 3VDUAL
GP15	STBY	H-Z	SPI_WP	STP_PCI#
GP16	MAIN	L OUT	DUAL BIOS CONTROL	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	H OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	VCC15_OV1	P/U 8.2K VCC3/X
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	VCC15_OV3	P/U 8.2K VCC3
GP22	MAIN	IN	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	TLS	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	MB_ID0	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	DUAL BIOS CONTROL	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT		
GP34	MAIN	OUT/LOW		N/A
GP35	MAIN	L OUT	400K FS CONTROL	N/A
GP36	MAIN	IN	DUAL BIOS CONTROL	P/U 8.2K VCC3
GP37	MAIN	IN	150K FS CONTROL	P/U 8.2K VCC3
GP38	MAIN	IN	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	VCORE_OV1	P/U 8.2K VCC3
GP49	MAIN	IN	STARPPING	P/D 8.2K

PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP50	MAIN	IN	REQ1#	
GP51	MAIN	IN	GNT1#	P/U 8.2K VCC3
GP52	MAIN	IN	REQ2#	P/U 8.2K VCC3
GP53	MAIN	IN	GNT2#	P/U 8.2K VCC3
GP54	MAIN	IN	REQ3#	P/U 8.2K VCC3
GP55	MAIN	IN	GNT3#	P/U 8.2K VCC3
GP56	STBY	IN	VCORE_OV5	
GP57	STBY	IN	VCORE_OV4	
GP58	STBY	IN	SPI_CS1#	
GP59	STBY		-USBOC_R	
GP60	STBY		LINKALRT#	

The diagram shows the TSM104 chip with several power and control pins connected to red circular components. VCC is connected to the top. VCC3_DAC is connected to a component labeled 'L'. VCC1_5 is connected to another component labeled 'L'. VGMCH_ME is connected to a third component labeled 'L'. DDR18V is connected to the bottom. A 5VSB input is connected to a converter block, which outputs VCC. A 5VDUAL input is connected to a converter block, which outputs 3VDUAL through an LDO1084 component.

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8718
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	ICH8
SYS FAN	FANPWM2	N/A	FANIO2	IT8718
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	ICH8
PWR FAN	N/A	N/A	FANIO3	IT8718
			ICH_FAN_TACH2	ICH8

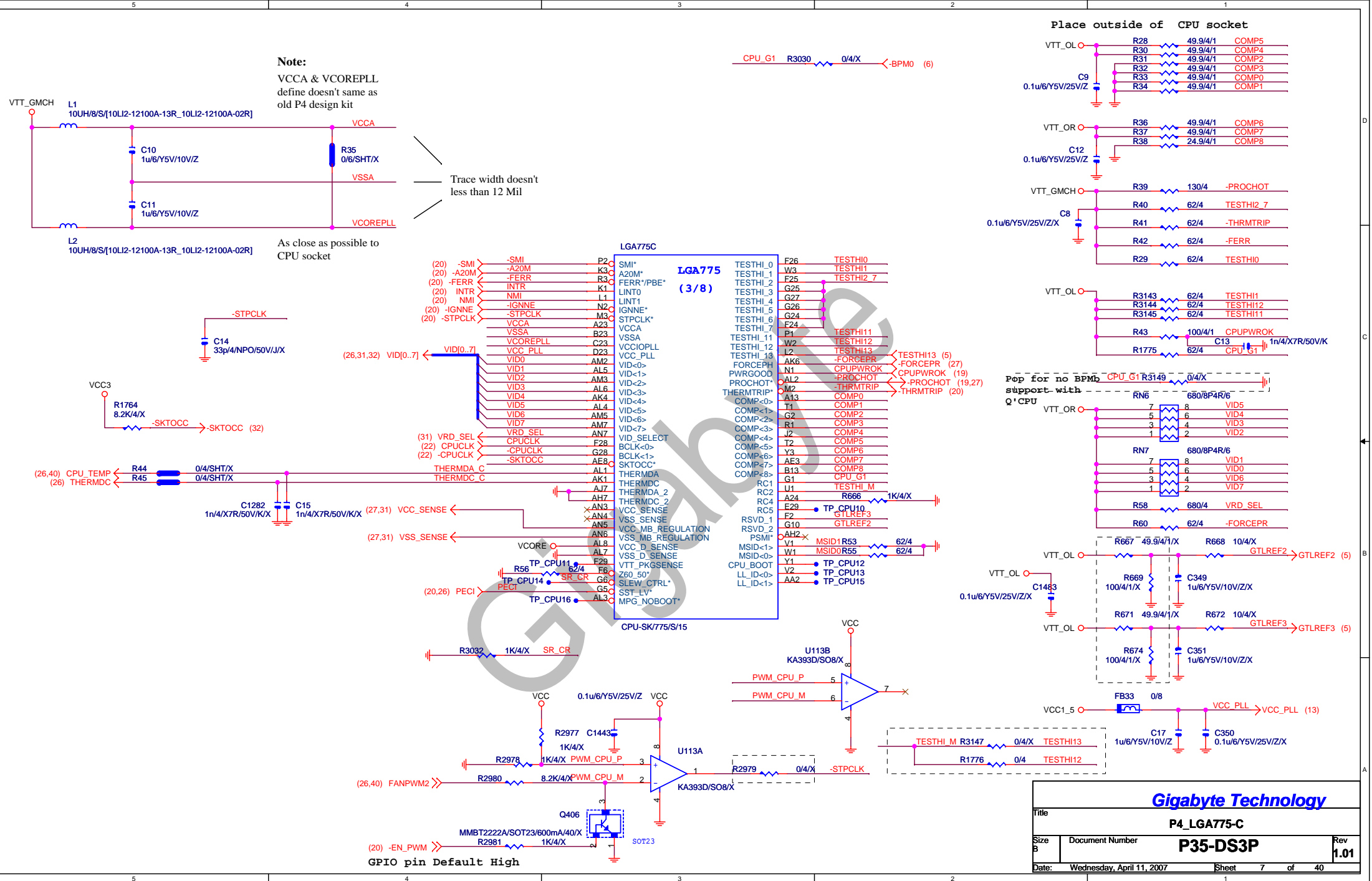
VCORE_OV5

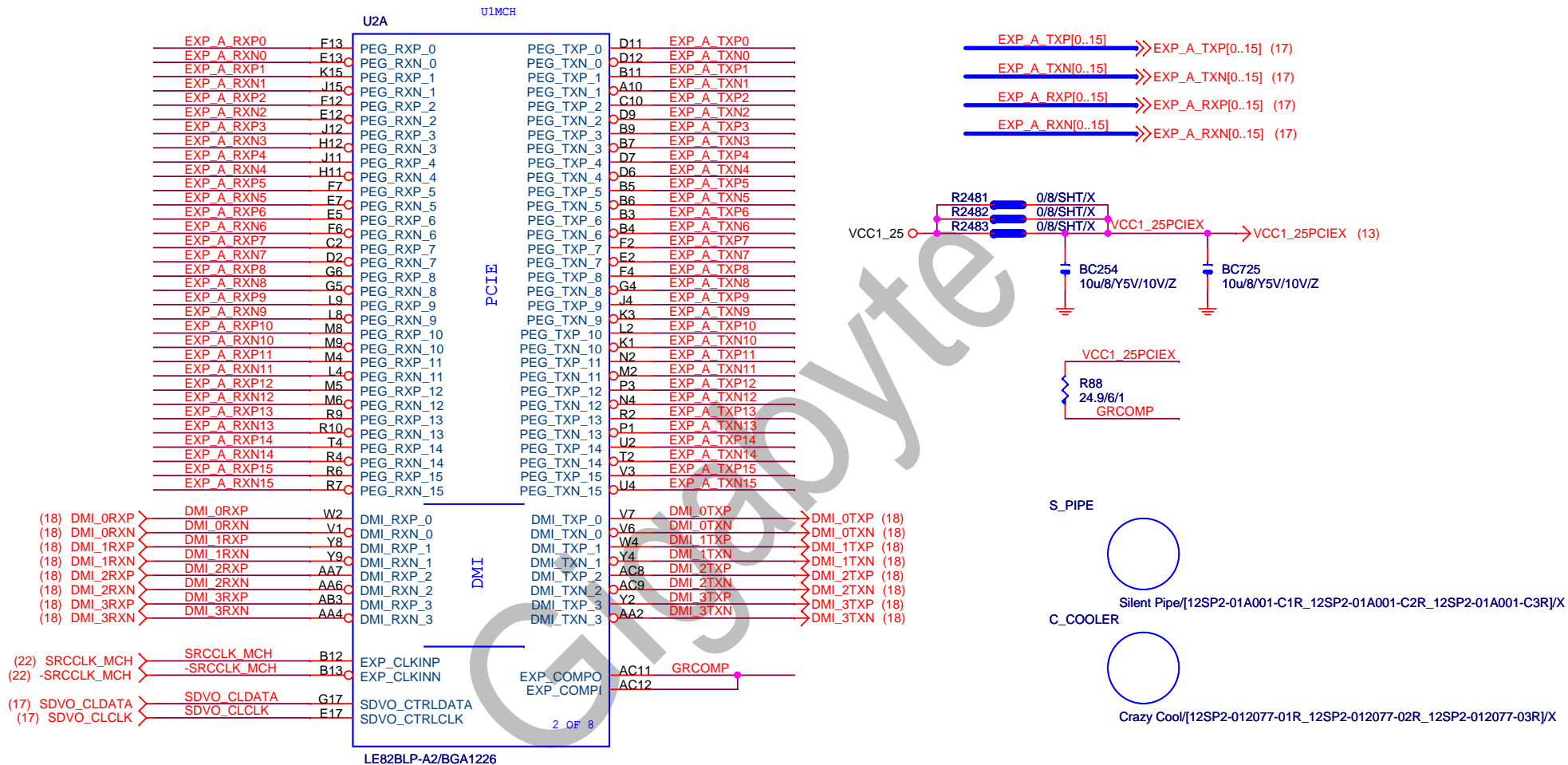
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TABLE LIST

Size B Document Number P35-DS3P Rev 1.01

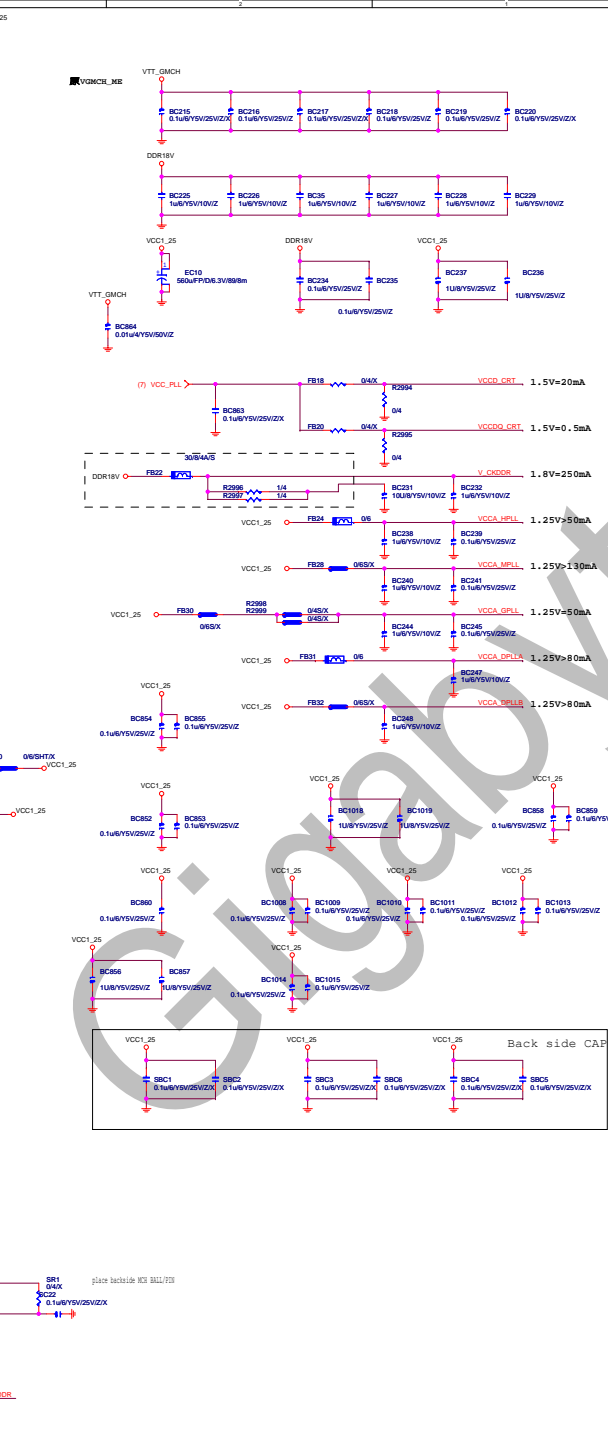
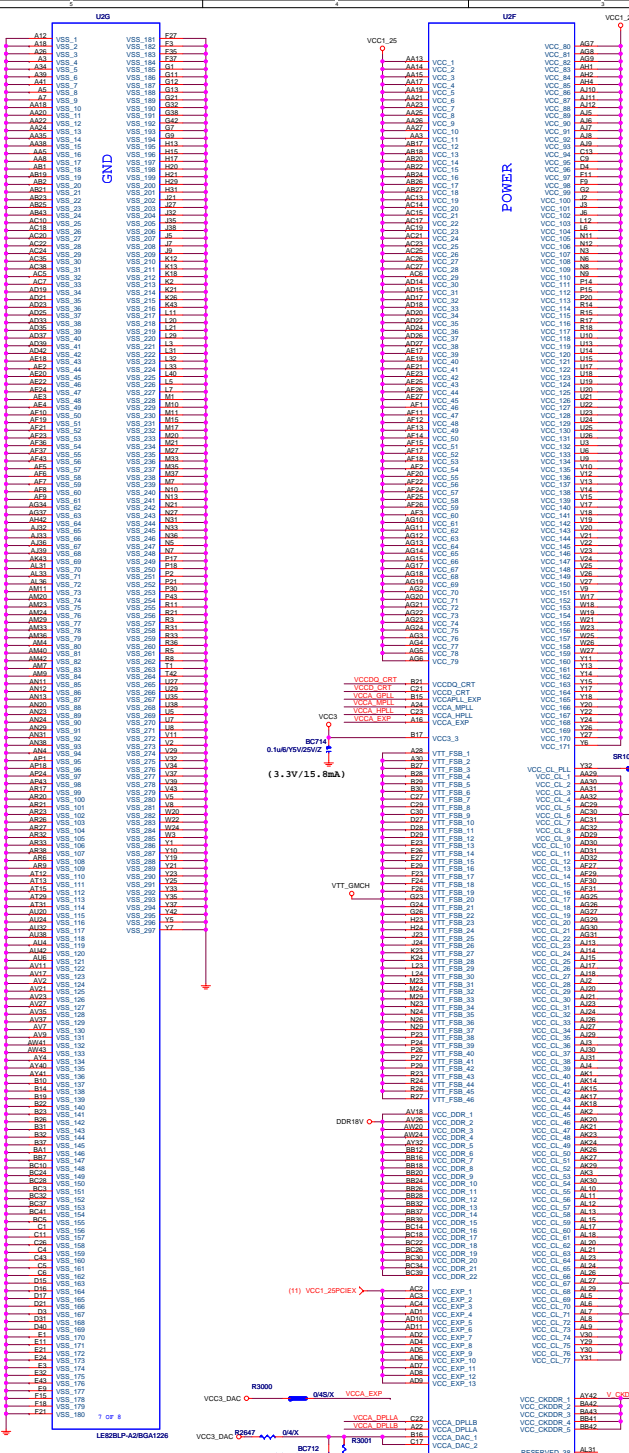
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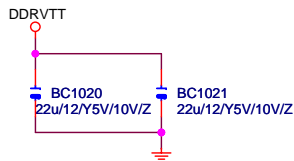
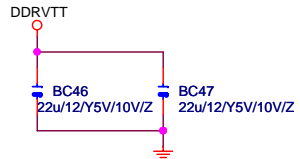
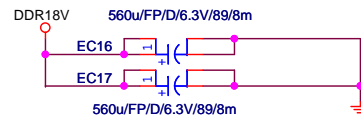
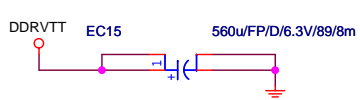
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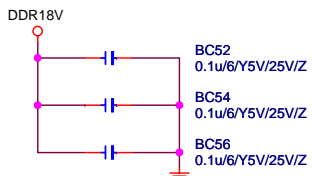


DDR TERMINATION CHANNEL A

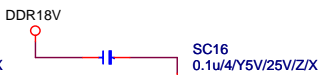
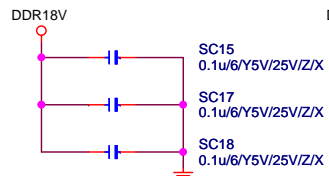
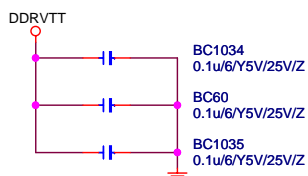
DDRVTT Decouple



DDR18V Decouple



DDRVTT Decouple



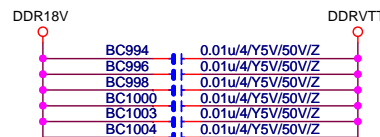
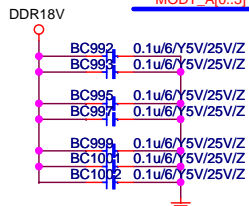
SBAA[0..2] ↔ SBAA[0..2] (10,14)

-CSA[0..3] ↔ -CSA[0..3] (10,14)

CKEA[0..3] ↔ CKEA[0..3] (10,14)

MAAA[0..14] ↔ MAAA[0..14] (10,14)

MODT_A[0..3] ↔ MODT_A[0..3] (10,14)



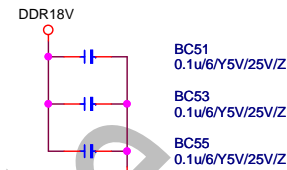
(10,14) -SCASA ↔ R165 33/4
(10,14) -SWEA ↔ R167 33/4
(10,14) -SRASA ↔ R169 33/4

MAAA5 R152 33/4
MAAA6 R154 33/4
MAAA9 R156 33/4
MAAA11 R158 33/4
MAAA12 R160 33/4
SBAA0 R162 33/4
MAAA14 R167 33/4

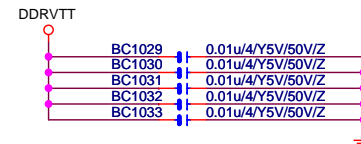
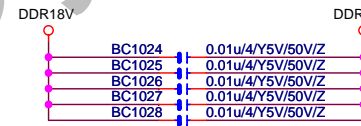
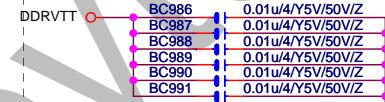
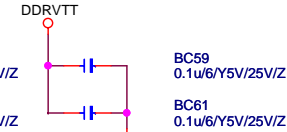
CSA0 R149 33/4
CSA1 R145 33/4
CSA2 R147 33/4
CSA3 R143 33/4
CKEA1 R141 33/4
CKEA2 R139 33/4
CKEA3 R137 33/4
CKEA0 R135 33/4
MAAA0 R133 33/4
MAAA10 R131 33/4
SBAA1 R129 33/4
MAAA13 R127 33/4
MAAA2 R125 33/4
MAAA1 R119 33/4
MAAA4 R117 33/4
MAAA7 R115 33/4
MAAA8 R113 33/4
MODT_A3 R161 33/4
MODT_A2 R162 33/4
MODT_A1 R163 33/4
MODT_A0 R161 33/4

DDR TERMINATION CHANNEL B

DDR18V Decouple



DDRVTT Decouple



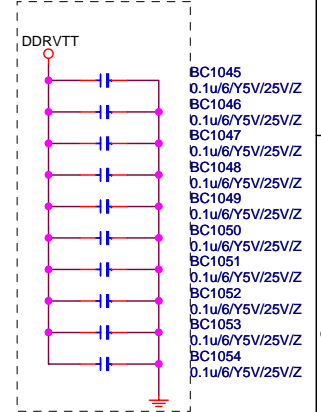
MODT_B[0..3] ↔ MODT_B[0..3] (10,15)

SBAB[0..2] ↔ SBAB[0..2] (10,15)

-CSB[0..3] ↔ -CSB[0..3] (10,15)

CKEB[0..3] ↔ CKEB[0..3] (10,15)

MAAB[0..14] ↔ MAAB[0..14] (10,15)



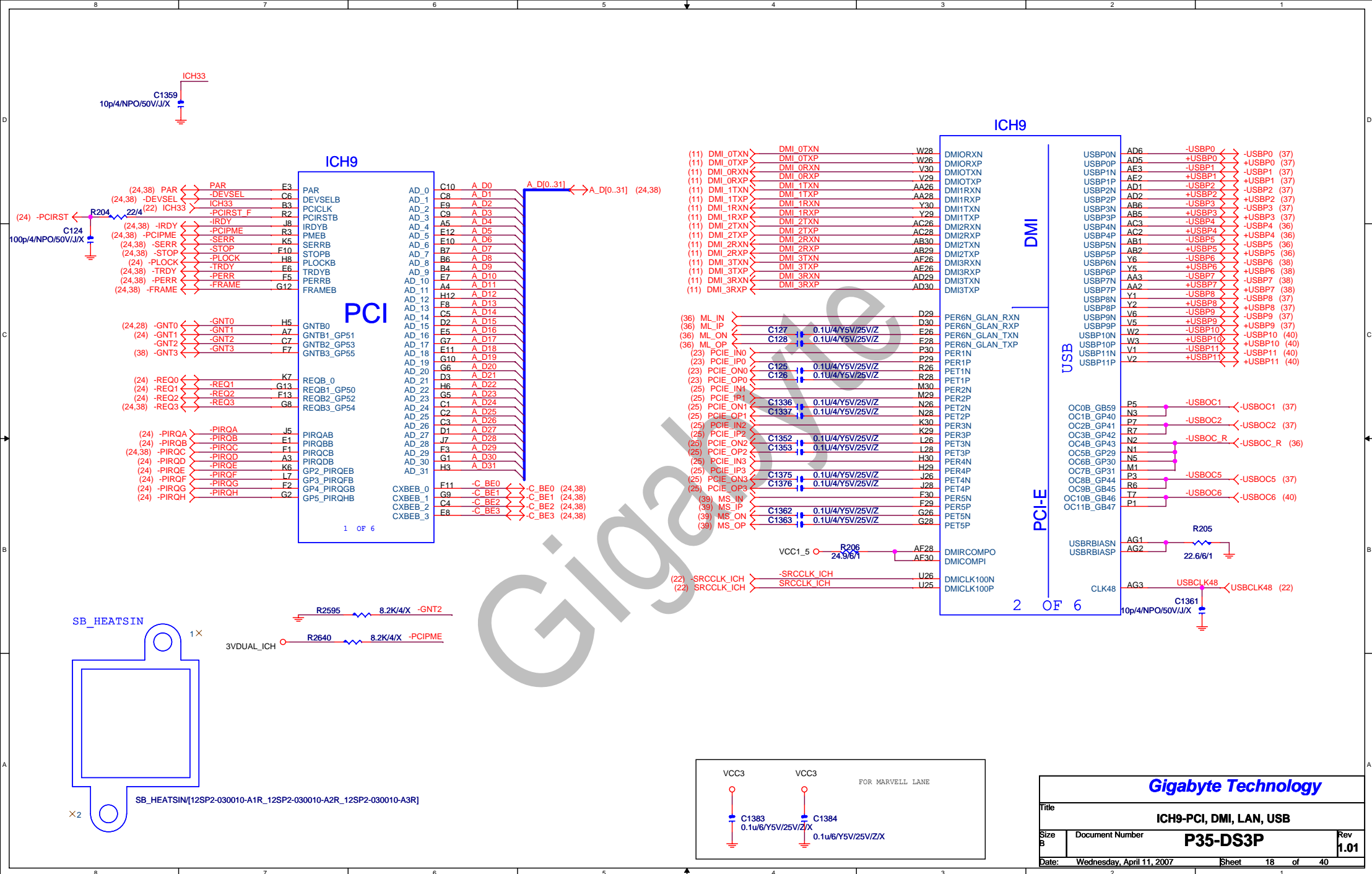
MAAB14 R167 33/4
MAAB1 R161 33/4
MAAB2 R161 33/4
MAAB4 R114 33/4
MAAB3 R116 33/4
MAAB5 R118 33/4
MAAB6 R120 33/4
MAAB13 R122 33/4
MAAB8 R124 33/4
MAAB7 R126 33/4
MAAB9 R128 33/4
MAAB11 R130 33/4
MAAB12 R162 33/4
MODT_B0 R134 33/4
MODT_B1 R136 33/4
MODT_B2 R138 33/4
MODT_B3 R140 33/4
SBAB1 R142 33/4
SBAB0 R144 33/4
MAAB10 R146 33/4
MAAB0 R148 33/4
CKEB0 R150 33/4
CKEB1 R151 33/4
CKEB3 R153 33/4
CKEB2 R155 33/4
-CSB3 R157 33/4
-CSB2 R159 33/4
-CSB1 R161 33/4
-CSB0 R163 33/4

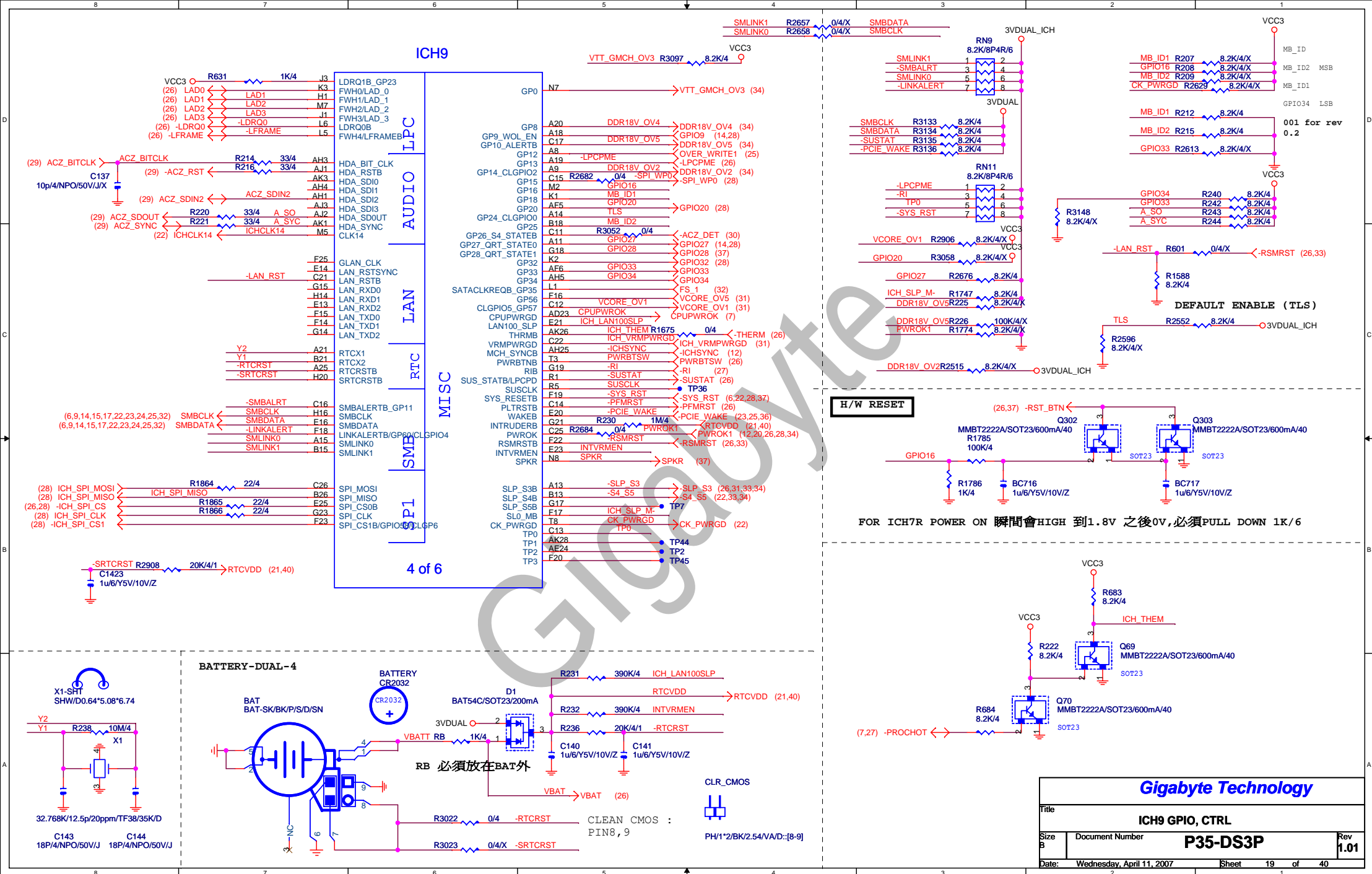
SBAB2 R164 33/4
R166 33/4
R168 33/4
R170 33/4
(10,15) -SWEA ↔ R165 33/4
(10,15) -SCASB ↔ R167 33/4
(10,15) -SRASB ↔ R169 33/4

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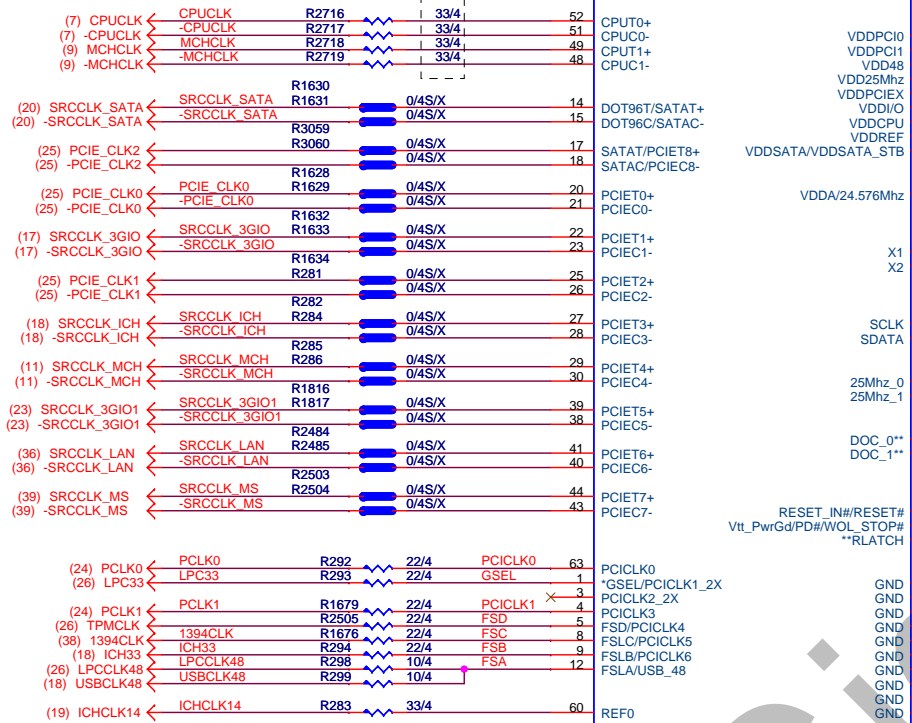
DDRII TERMINATOR

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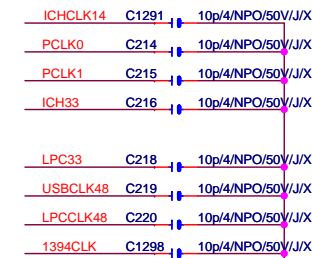
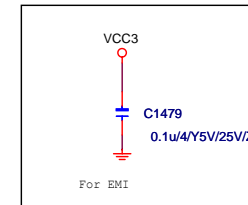
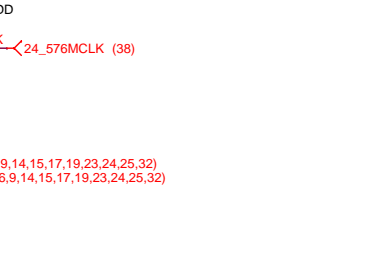
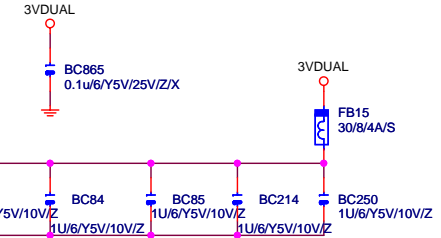
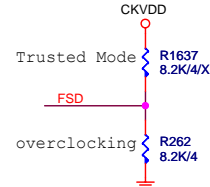
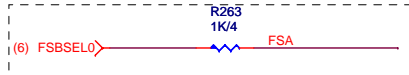
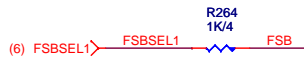


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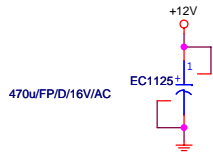


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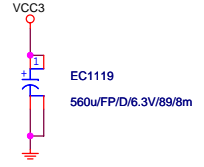
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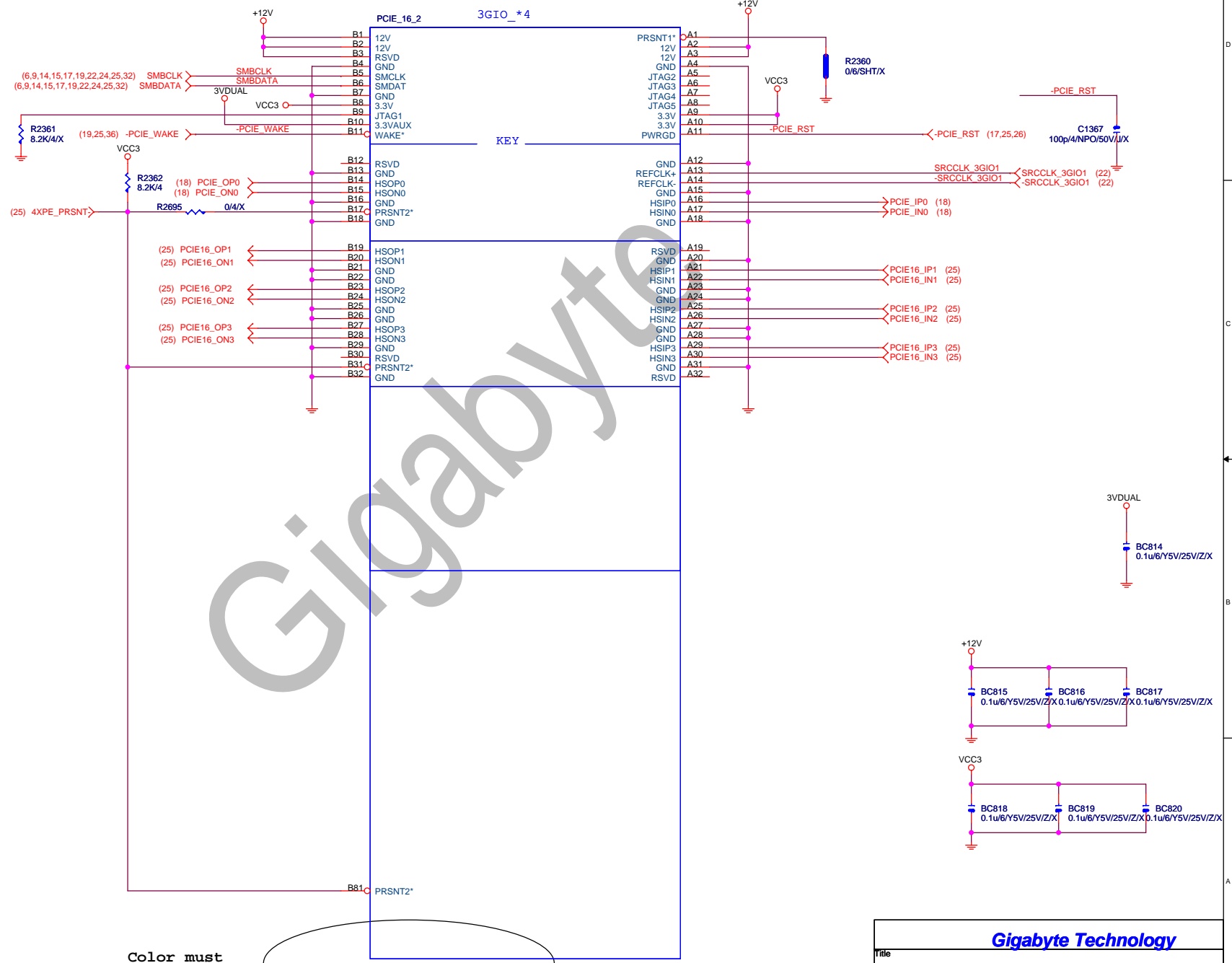
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470uF/FP/D/16V/AC



EC1119
560uF/FP/D/6.3V/89/8m



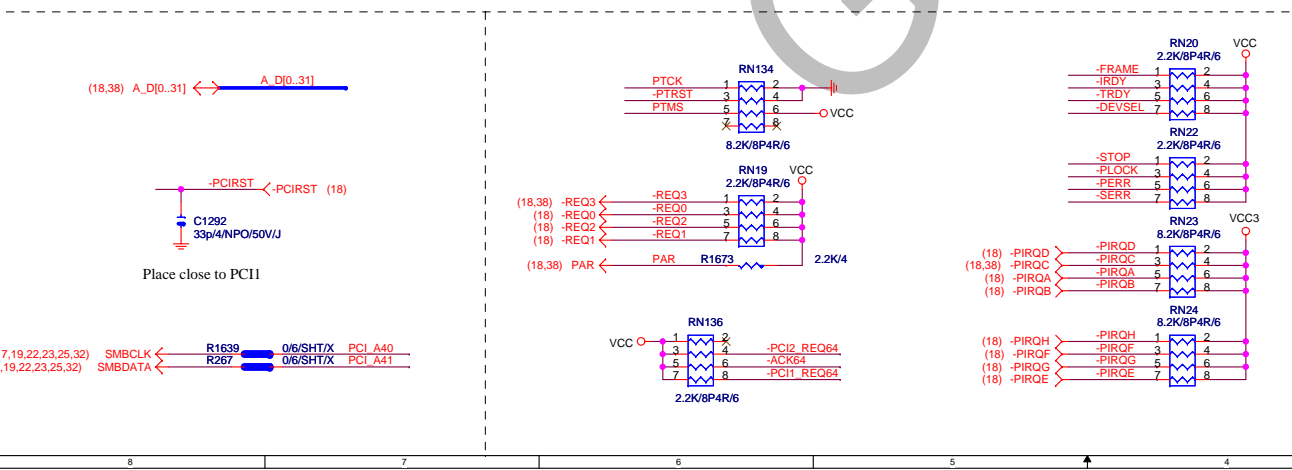
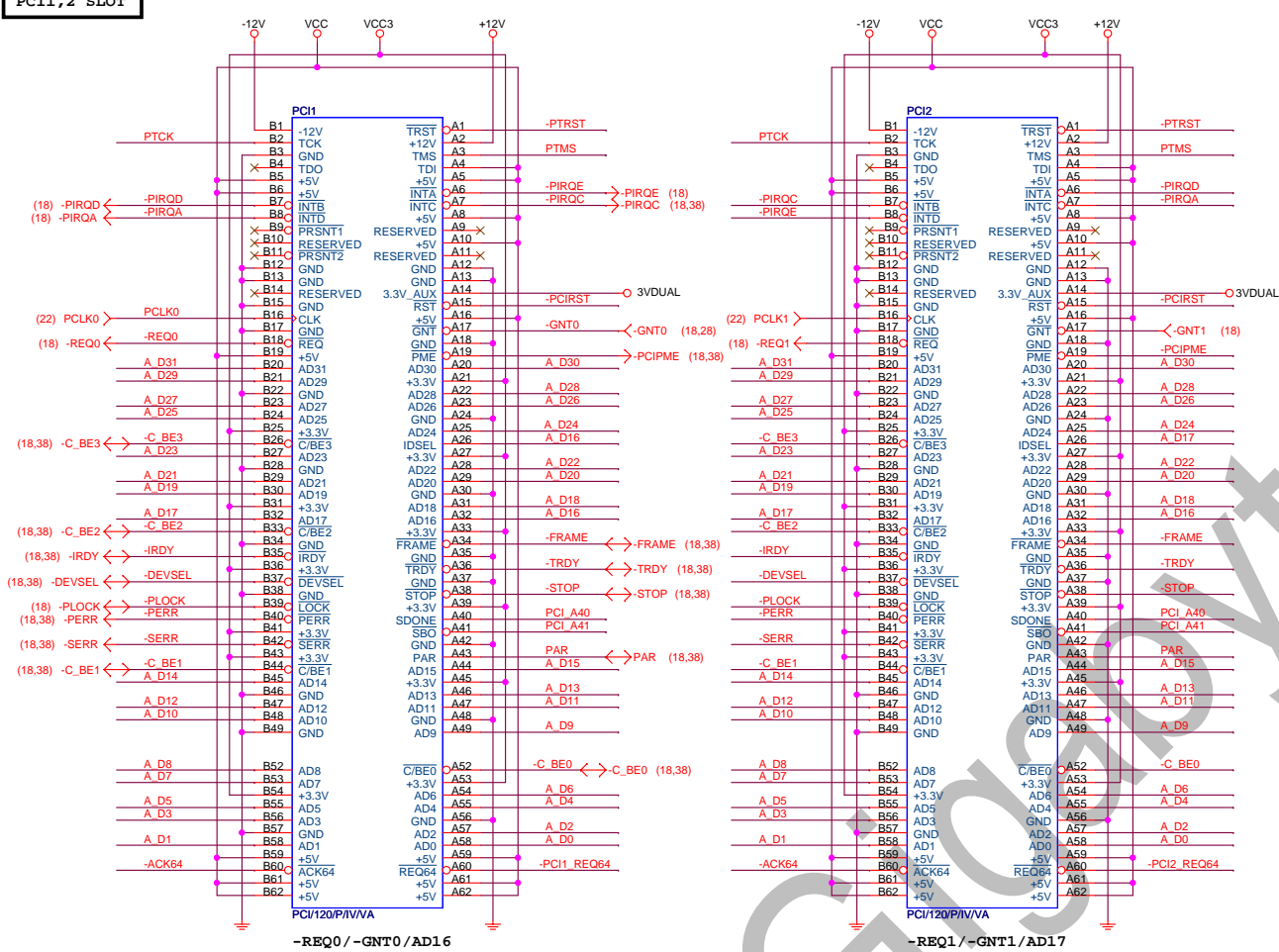
Color must
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PCI-E/16X-65P/OR/RIGHT PUSH

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PCI EXPRESS X 4 PORT			
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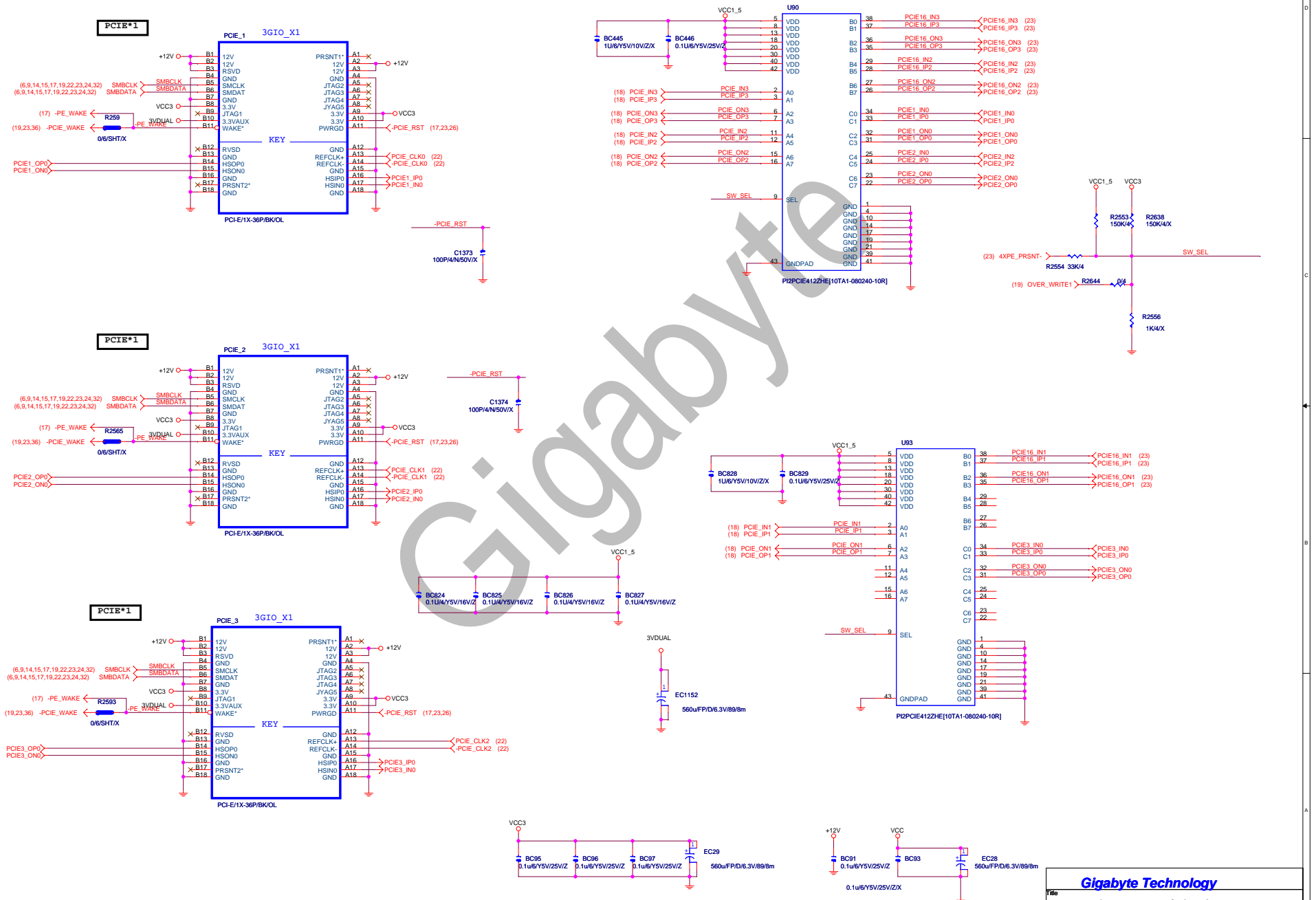
PCI1,2 SLOT

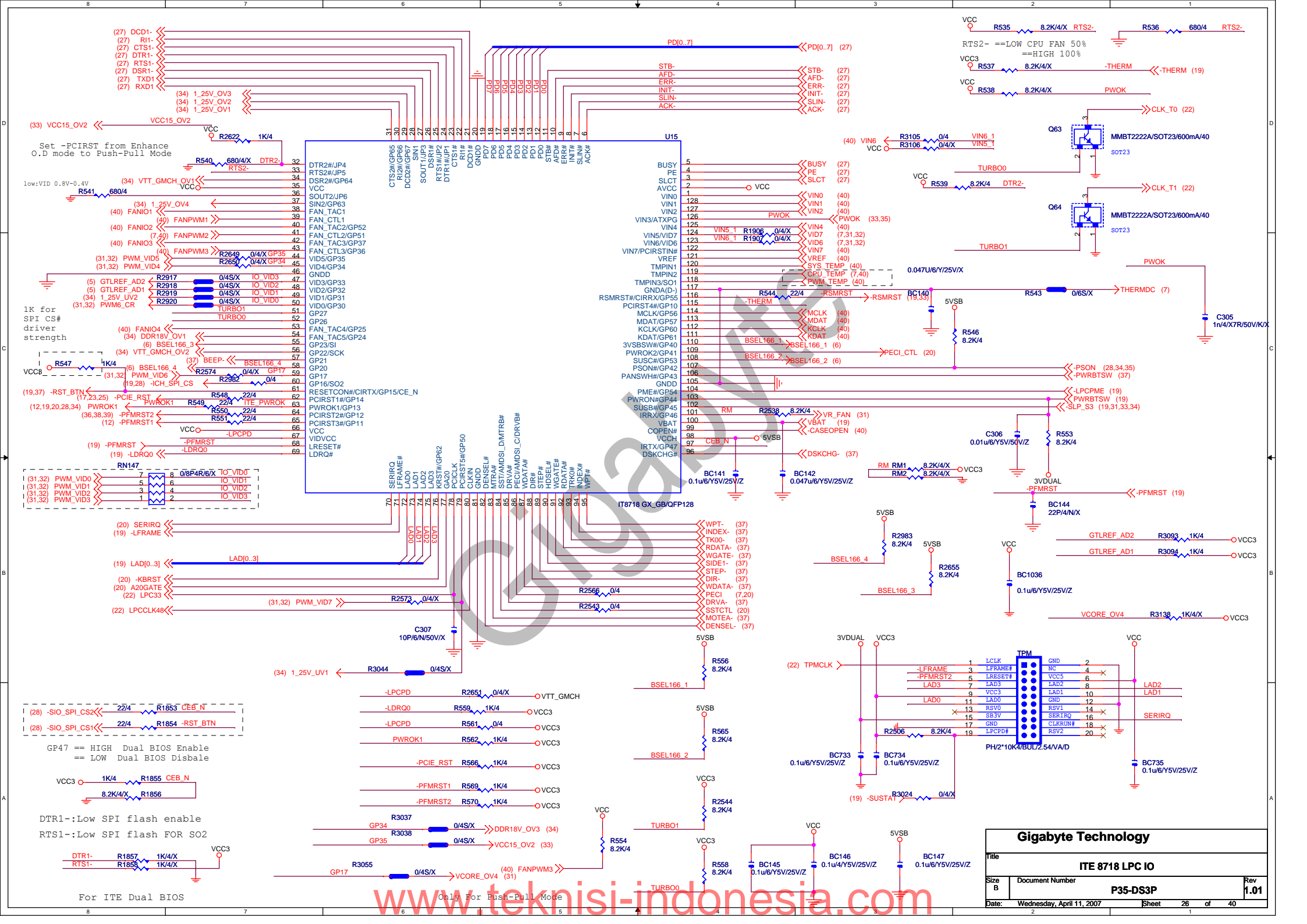


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PCI SLOT 1, 2			
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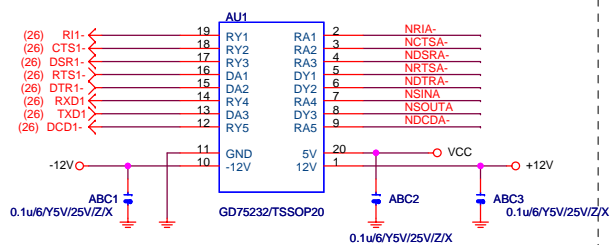
L : A-B (X4 X1)
H : A-C (X1 X4)

For Vih level consideration



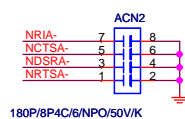
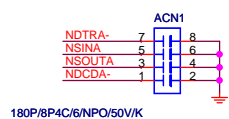
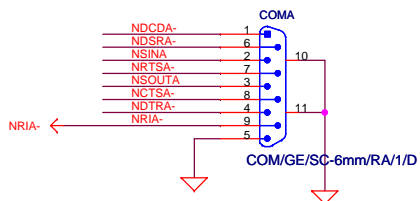
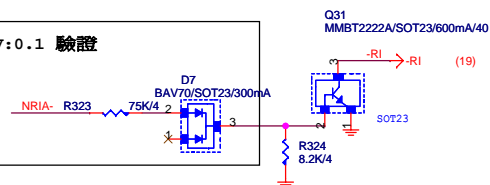


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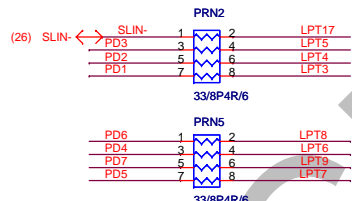
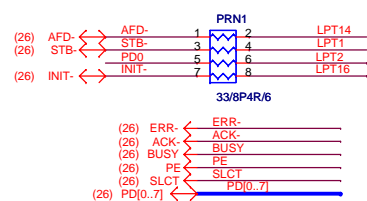


COM RI

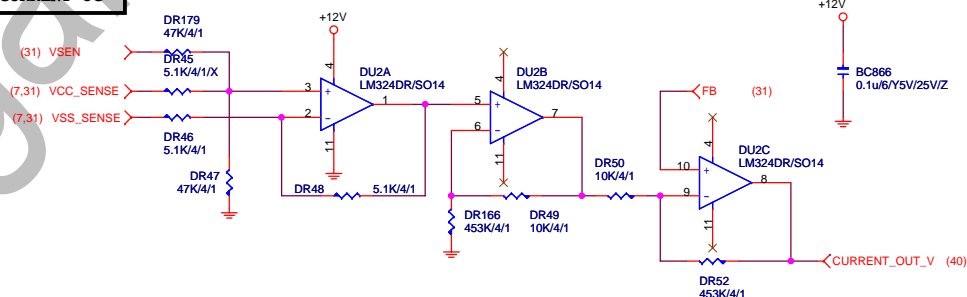
REV:0.1 驗證



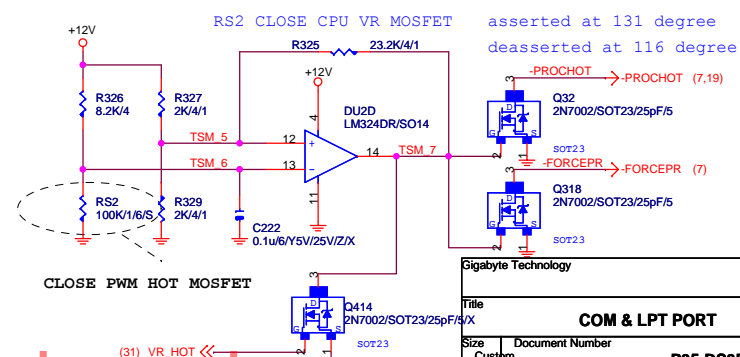
LPT PORT



DYNAMIC CURRENT OC

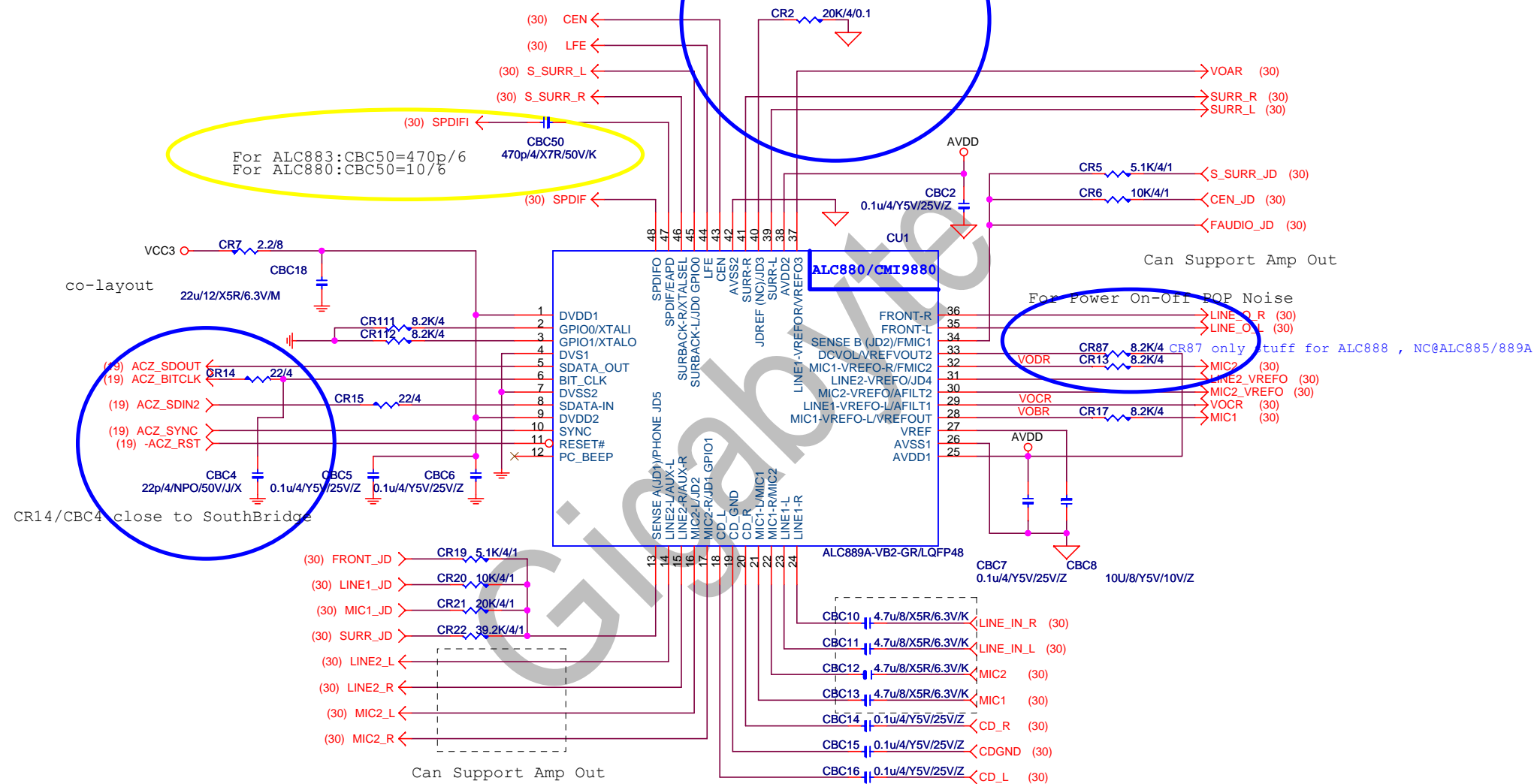


-PROHOT



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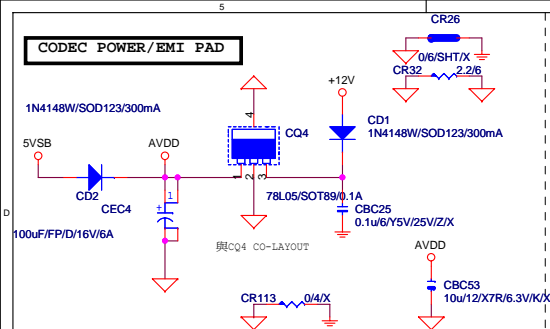
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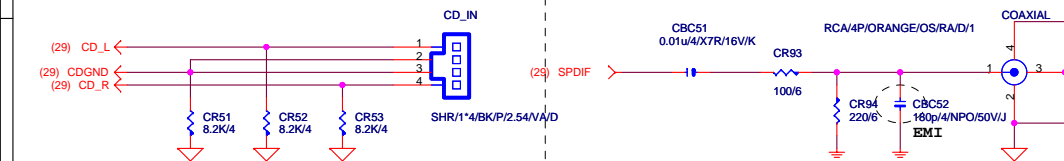
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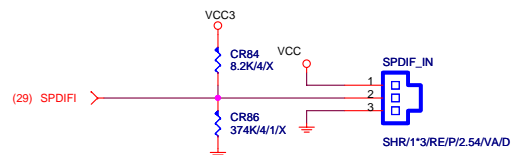
CODEC POWER/EMI PAD



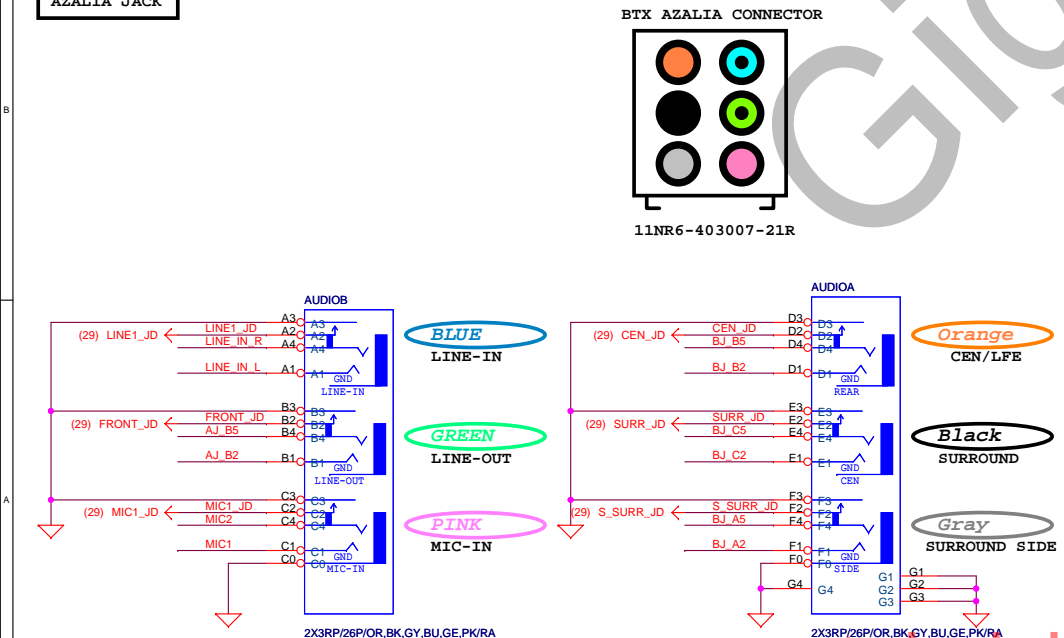
CD IN



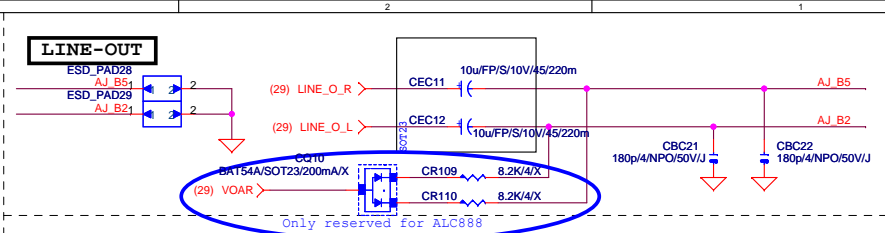
SPDIF



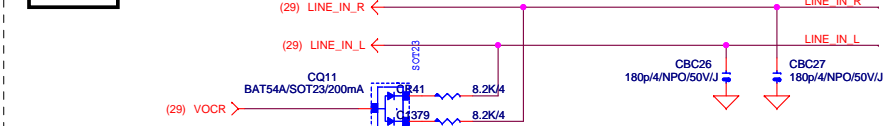
AZALIA JACK



LINE-OUT



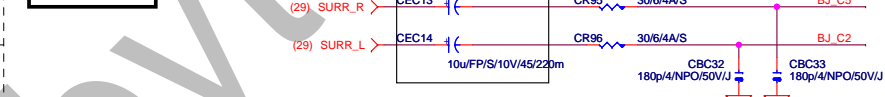
LINE-IN



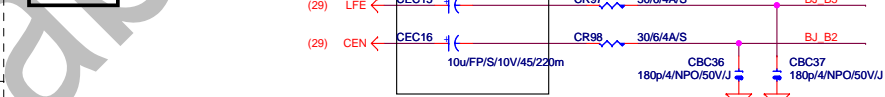
MIC-IN



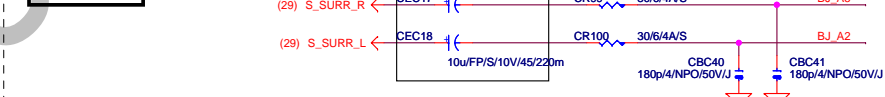
SURROUND



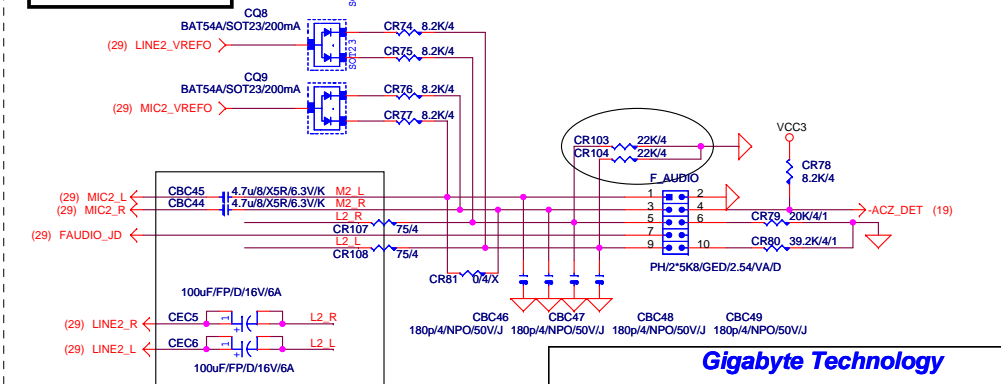
CEN/LFE



SURR BACK

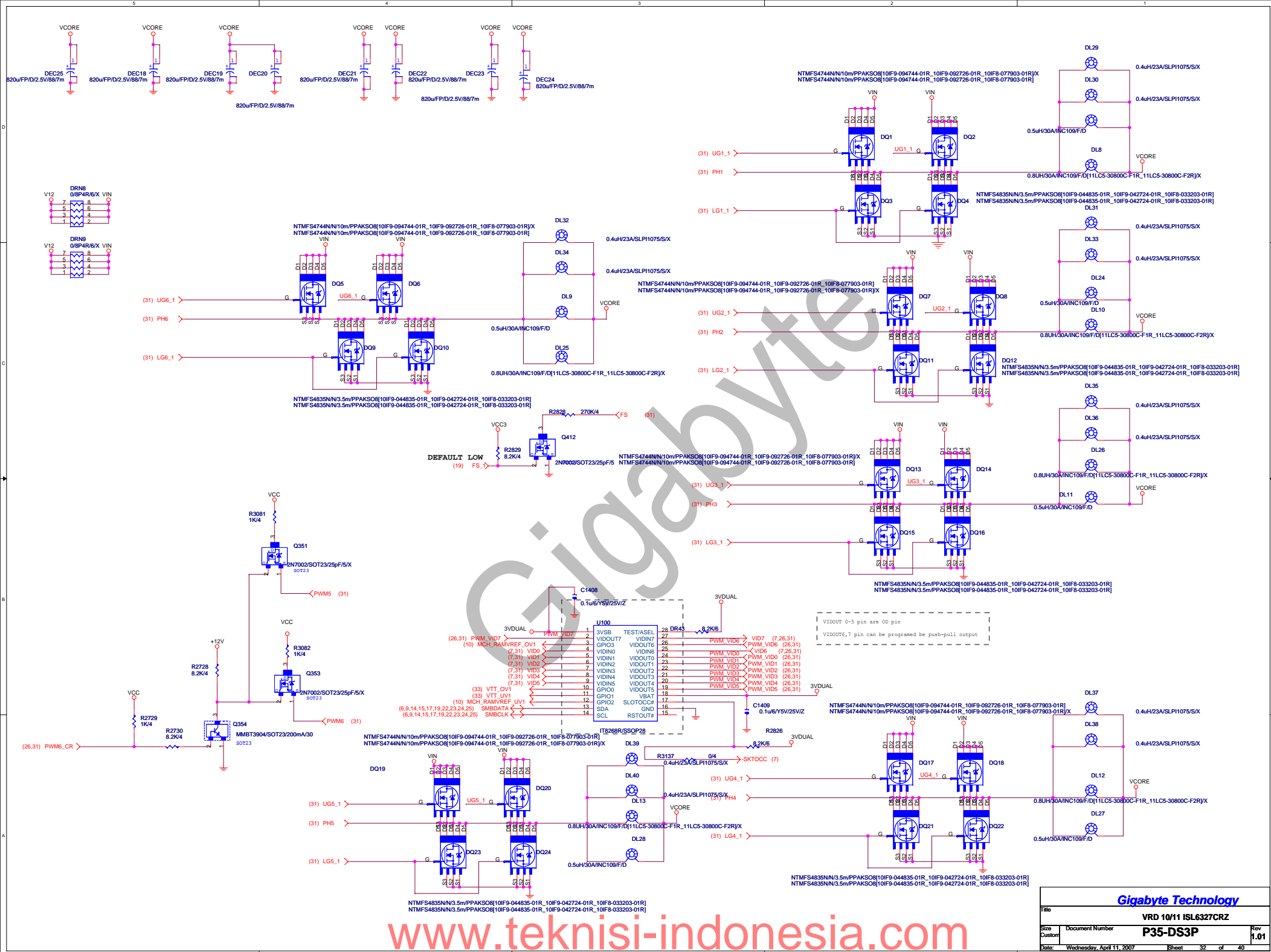


AZALIA FRONT PANEL



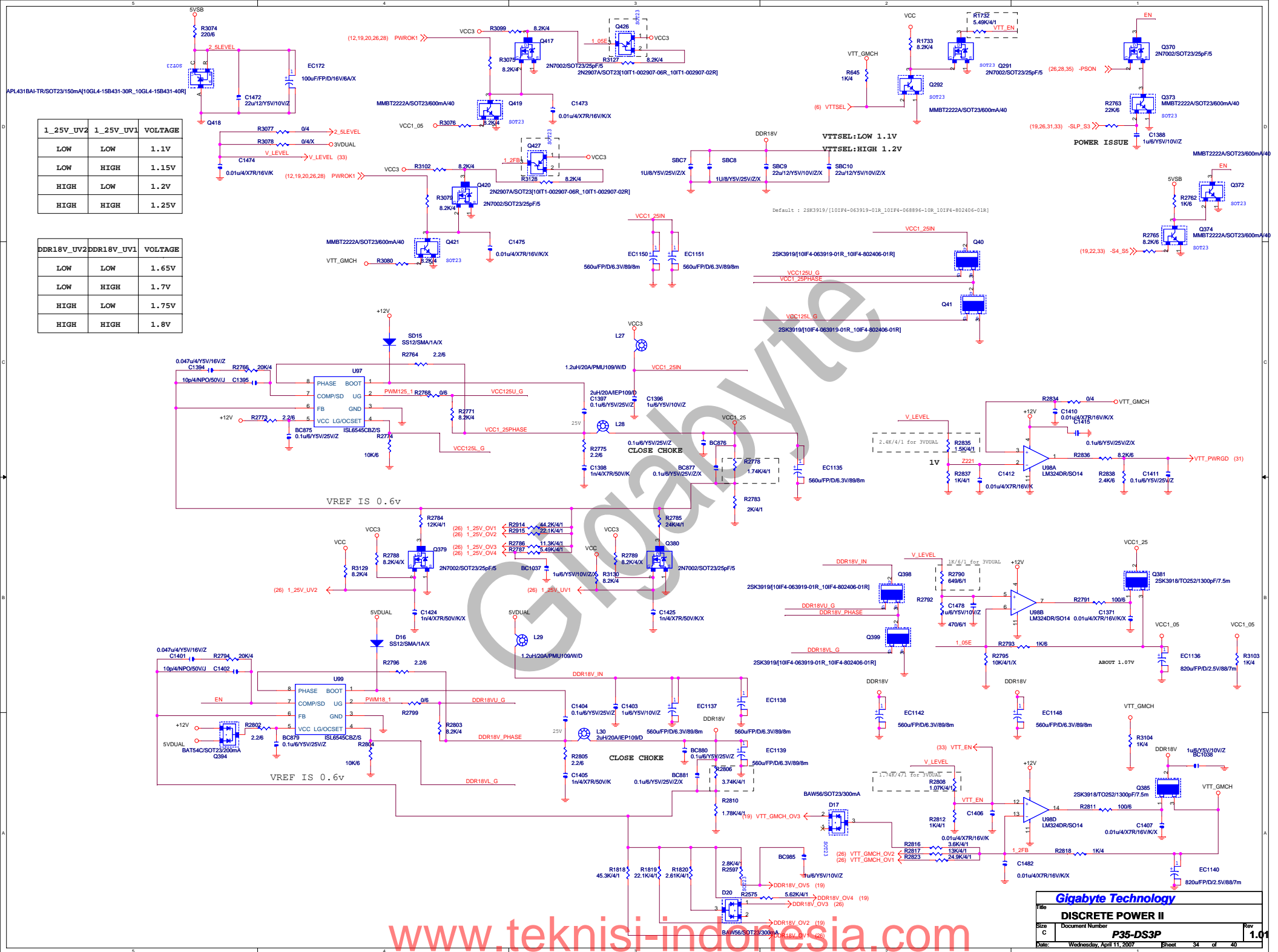
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1_25V_UV2	1_25V_UV1	VOLTAGE
LOW	LOW	1.1V
LOW	HIGH	1.15V
HIGH	LOW	1.2V
HIGH	HIGH	1.25V

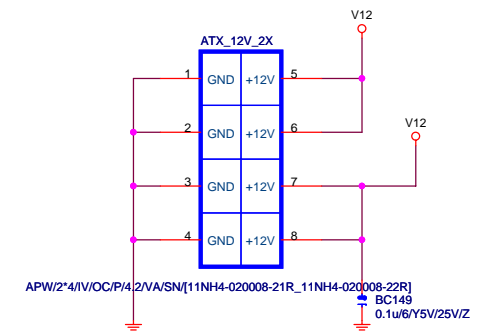
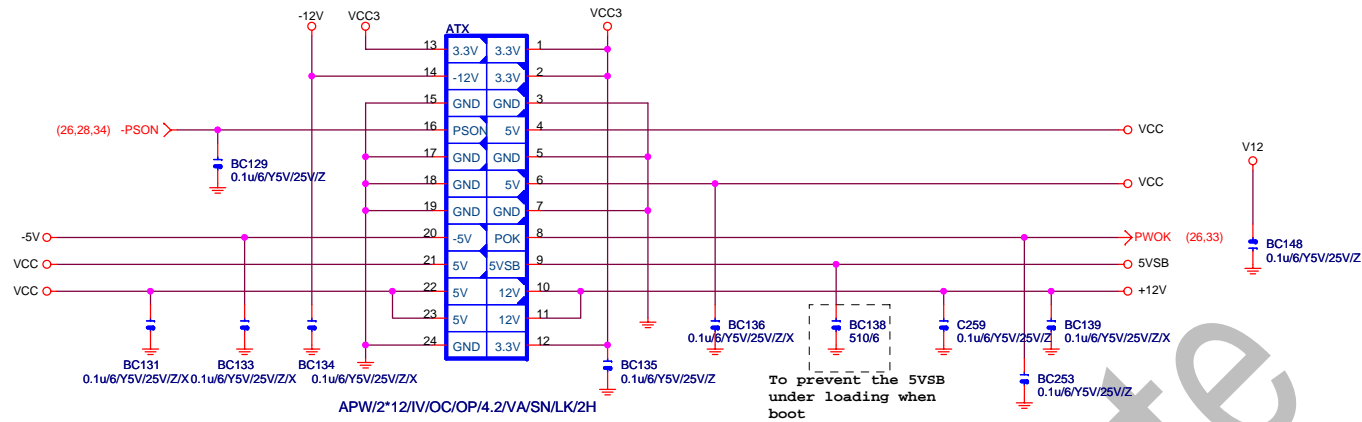
DDR18V_UV2	DDR18V_UV1	VOLTAGE
LOW	LOW	1.65V
LOW	HIGH	1.7V
HIGH	LOW	1.75V
HIGH	HIGH	1.8V



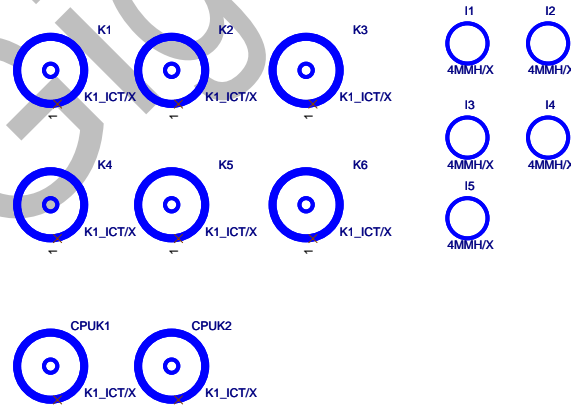
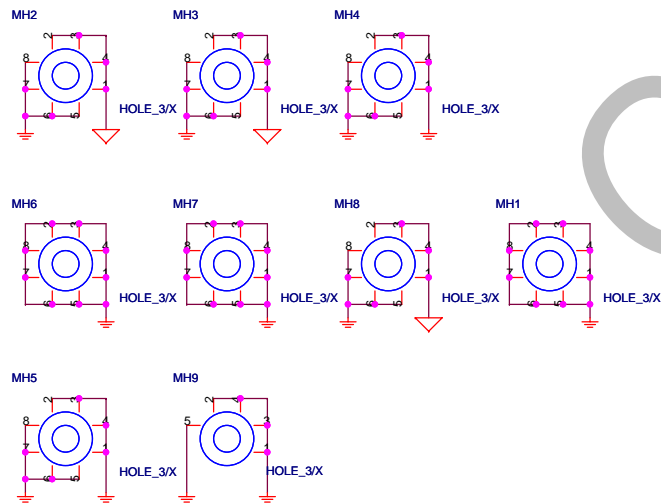
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DISCRETE POWER II			
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ATX POWER CONNECTOR

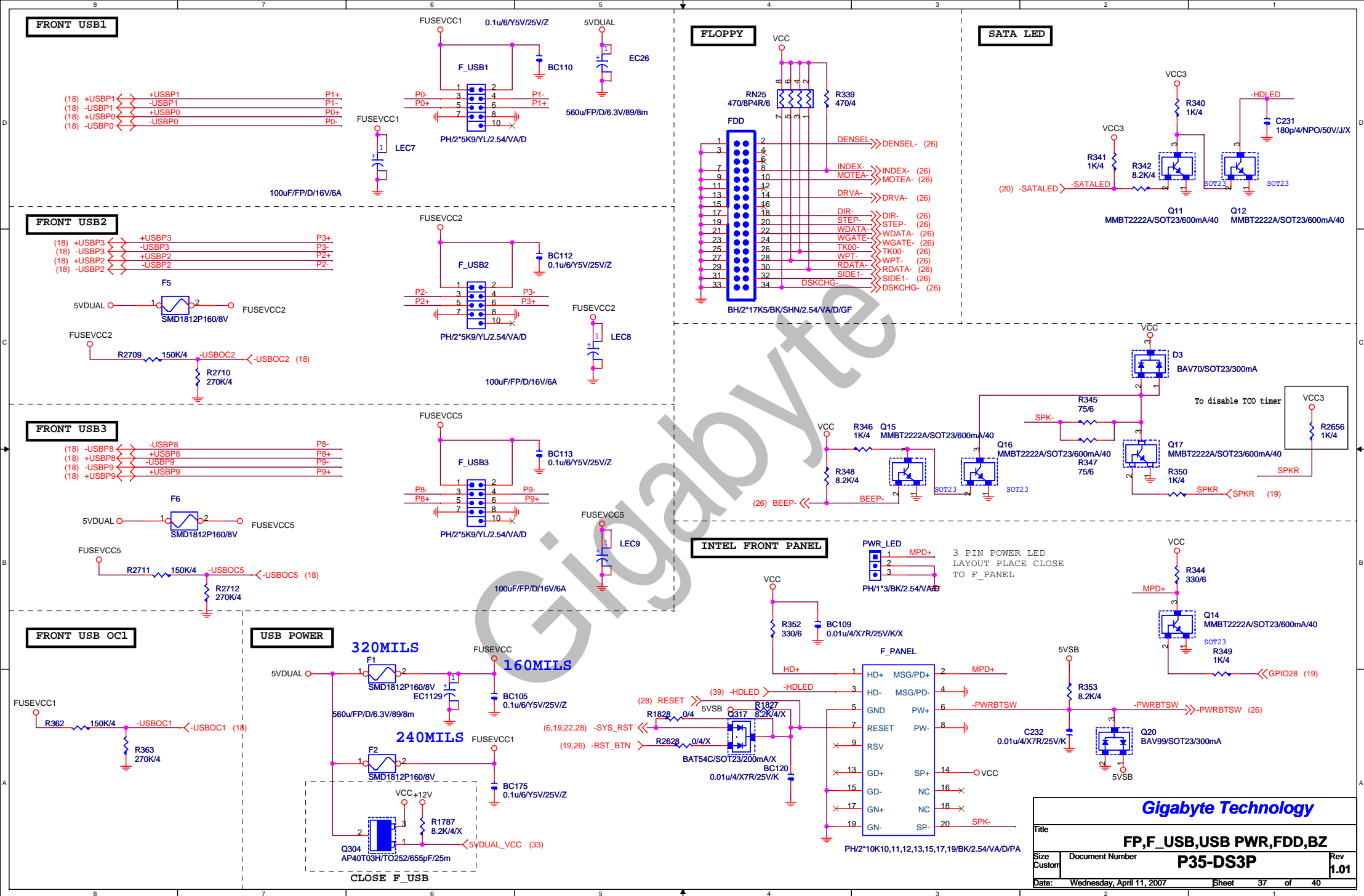


HOLE_3-2--->有鉛



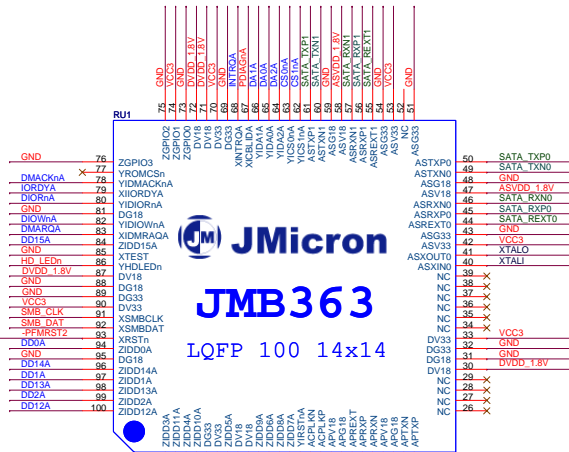
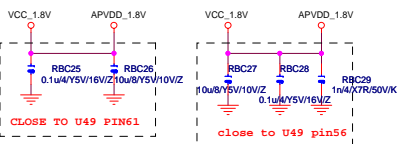
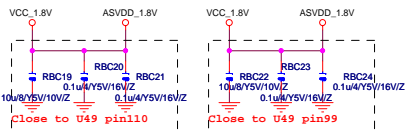
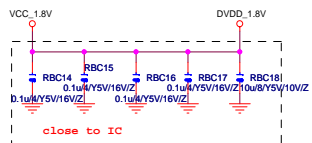
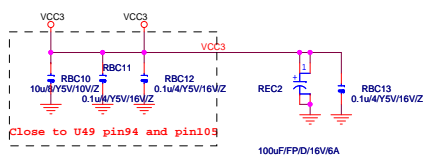
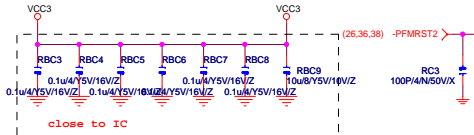
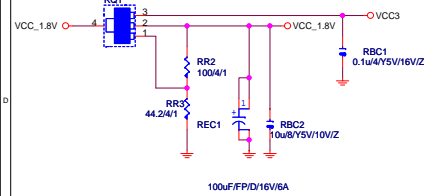
Gigabyte Technology

Title		
ATX POWER CONNECTOR		
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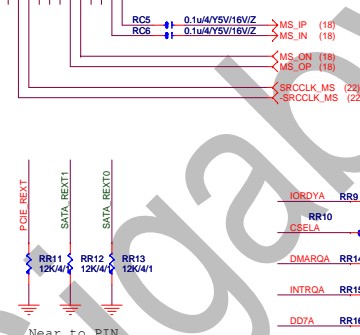
3.3V to 1.8V Voltage Regulator

AMC11175K/SOT223/0.8A[IGL3-08117-06R]

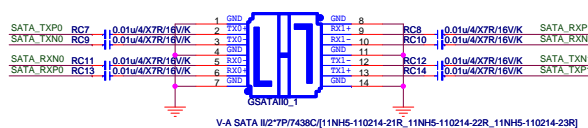


JMicron
JMB363
LQFP 100 14x14

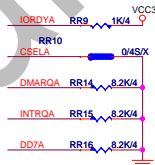
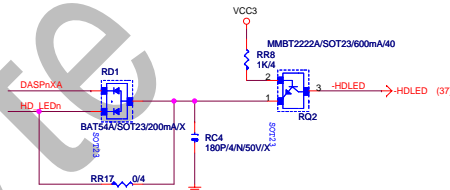
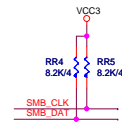
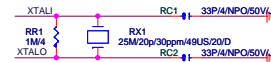
GBB636LQFP100[10HP2-640363-20R]



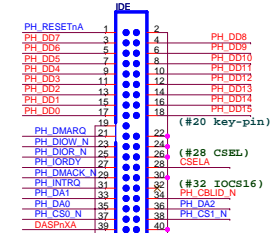
SATA Connector



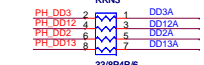
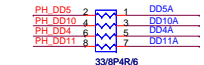
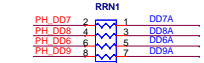
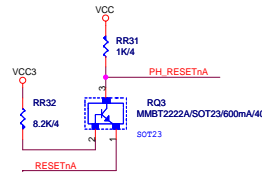
V-A SATA I/27P/7438C[11NH5-110214-21R, 11NH5-110214-22R, 11NH5-110214-23R]



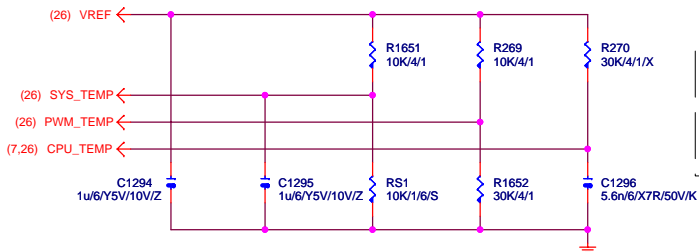
IDE Connector



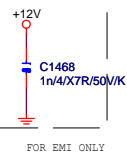
BH2720K20/GEL/2.54RA/DGF[11NR3-010220-D1R, 11NR3-010220-D2R]



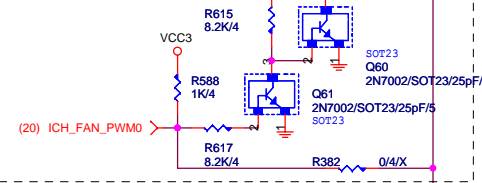
TEMP H/W MONITOR



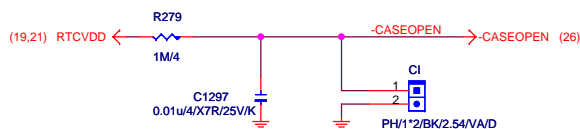
CPU SMART FAN



ICH8 FAN CTRL

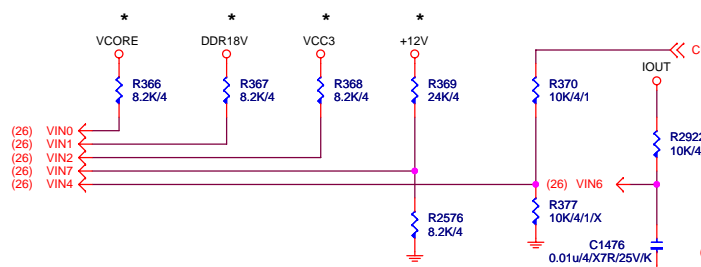


CASE OPEN

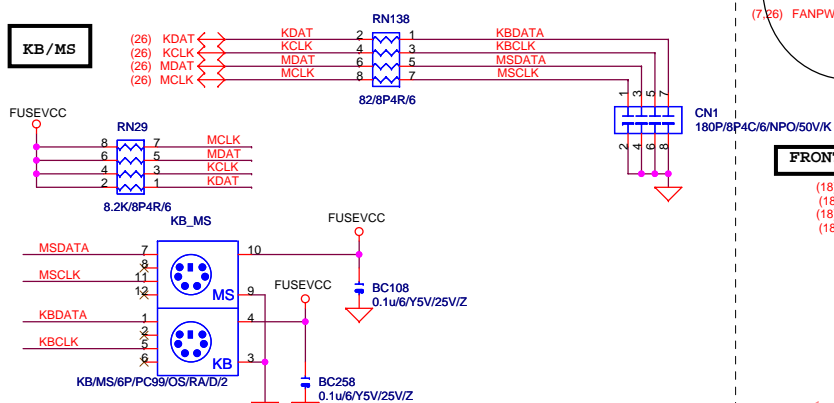


Case Open Circuits

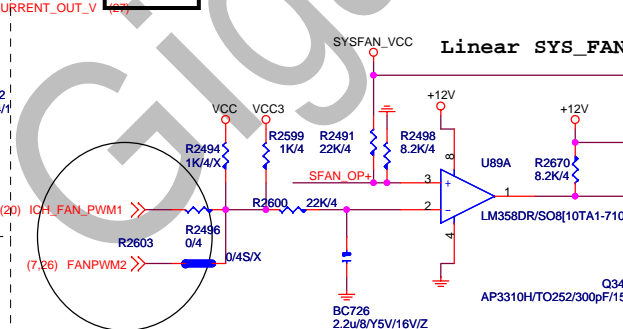
VOLTAGE-- H/W MONITOR



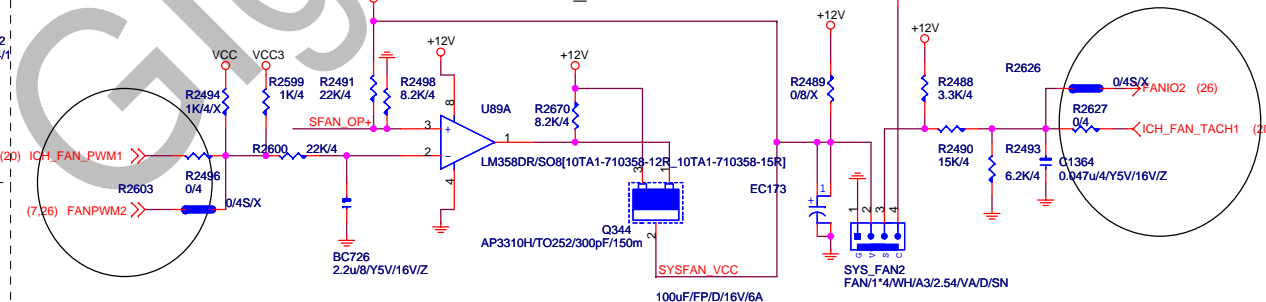
KB/MS



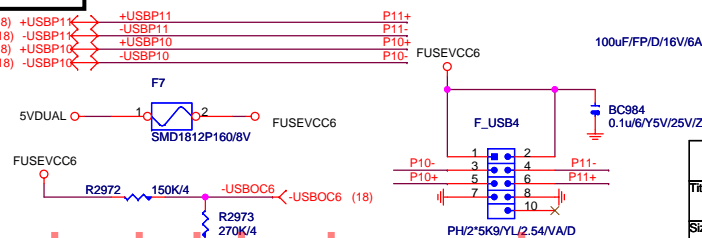
SYS FAN



Linear SYS_FAN



FRONT USB2



Gigabyte Technology

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